UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Katsumi Sameshima

Serial No.: 09/451,979

Filed: November 30, 1999

For: FERROELECTRIC MEMORY AND METHOD FOR MANUFACTURING SAME

Commissioner for Patents
Washington, D.C. 20231

Examiner: Wai-Sing Louie

Group Art Unit: 2814

Docket: 362-39 RCE

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Dated: February 21, 2003

I hereby certify this correspondence is being deposited with the United States Postal Service as first class mail, postpaid in an envelope, addressed to: Commissioner for Patents, Washington, D.C. 20231 on February 21, 2003
Signature: Marguerite Franco
Marguerite Franco

REPLY TO FINAL OFFICE ACTION

Sir:

In response to the Office Action mailed October 21, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend Claims 2 and 3 by rewriting the same as follows:

2. (Thrice Amended) A ferroelectric memory, comprising:

an insulation film having a hollow at a top surface; and

a laminated body obtained by laminating a plurality of layers on said top surface and etching a region of said plurality of layers corresponding to a region other than said hollow, wherein said laminated body includes a lower electrode layer, a ferroelectric layer formed on said lower electrode layer and an upper electrode layer formed on said ferroelectric layer; and the memory further comprising another film embedded from said top surface of said insulation film in a position of a predetermined depth, exposed only at a bottom of said